WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a field isolation layer formed on a semiconductor substrate to define an active region;

gate patterns formed on the active region;

source regions formed in the active region between the gate patterns;

a conductive pattern connecting the source regions and being interposed between the gate patterns; and

a resistor formed on the field isolation layer,

wherein the conductive pattern and the resistor are formed of the same material.

2. The semiconductor device as claimed in claim 1, wherein the conductive pattern and the resistor are formed of polysilicon.

3. The semiconductor device as claimed in claim 1, wherein the gate pattern comprises a tunnel insulation layer, a charge trapping layer, a blocking insulation layer, and a gate electrode that are sequentially stacked on the semiconductor substrate.

4. The semiconductor device as claimed in claim 3, wherein the tunnel insulation layer and the blocking insulation layer are formed of oxide.

5. The semiconductor device as claimed in claim 3, wherein the charge trapping layer is formed of nitride.

6. The semiconductor device as claimed in claim 3, wherein the gate electrode comprises a polysilicon layer and a metal silicide layer that are sequentially stacked.

7. The semiconductor device as claimed in claim 1, wherein the conductive pattern and the resistor are horizontally aligned.

8. The semiconductor device as claimed in claim 1, further comprising spacers covering sidewalls of the gate pattern.

9. The semiconductor device as claimed in claim 8, wherein the spacers are formed of nitride or oxide.

10. The semiconductor device as claimed in claim 1, further comprising a dummy gate pattern on the field isolation layer adjacent to the resistor.

11. A method of forming a semiconductor device, the method comprising:

forming a field isolation layer to define an active region at a semiconductor substrate;

sequentially forming a gate insulation layer and a gate conductive layer on the surface of the semiconductor substrate where the field isolation layer is formed;

sequentially patterning the gate conductive layer and the gate insulation layer to form a gate pattern including a gate insulation pattern and a gate conductive pattern on the active region;

implanting impurities into the active region between the gate patterns, using the gate patterns as ion-implantation masks to form a source region; and

forming a conductive pattern connecting the source regions and simultaneously forming a resistor on the field isolation layer.

12. The method as claimed in claim 11, wherein the conductive layer is formed of polysilicon.

13. The method as claimed in claim 11, wherein the gate insulation layer comprises a tunnel insulation layer, a charge trapping layer, and a blocking insulation layer that are sequentially stacked.

14. The method as claimed in claim 13, wherein the tunnel insulation layer and the blocking insulation layer are formed of oxide.

15. The method as claimed in claim 13, wherein the charge trapping layer is formed of nitride.

16. The method as claimed in claim 11, wherein the gate conductive layer comprises a polysilicon and a metal silicide that are sequentially stacked.

17. The method as claimed in claim 11, further comprising forming a dummy gate pattern on the field isolation layer when forming the gate pattern on the active region.

18. The method as claimed in claim 11, after forming the source region, further comprising forming spacers covering sidewalls of the gate pattern.

19. The method as claimed in claim 18, wherein the spacers are formed of oxide or nitride.

20. A method of forming a semiconductor device, the method comprising:

defining an active region at a semiconductor substrate;

implanting impurities into selective areas of the active region to form source regions; and

forming a conductive pattern connecting the source regions and simultaneously forming a resistor, said conductive pattern and said resistor being formed of the same material.

21. The method of forming a semiconductor device of claim 20, wherein a field isolation layer is used to define said active region.

22. The method of forming a semiconductor device as recited in claim 20, further comprising sequentially forming a gate insulating layer and a gate conductive layer on said semiconductor substrate.

23. The method recited in claim 20, wherein said conductive pattern and said resistor are formed of polysilicon.

24. A semiconductor device comprising;

an active region on a semiconductor substrate;

source regions in said active region;

a conductive pattern connecting said source regions; and

a resistor, wherein said conductive pattern and said resistor are formed of the same material.

25. The semiconductor device of claim 24, wherein a field isolation layer formed on a semiconductor substrate defines said active region.

26. The semiconductor device of claim 24, further comprising gate patterns formed on said active region.

27. The semiconductor device of claim 26, wherein said source regions are formed in the active region between said gate patterns.

28. The device recited in claim 24, wherein said conductive pattern and said resistor are formed of polysilicon.